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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,930	06/07/2000	Brian A. Day	1003-0549	8543

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EXAMINER

TORRES, JOSEPH D

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 12/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/589,930	DAY, BRIAN A.
	Examiner Joseph D. Torres	Art Unit 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 07 June 2000.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-12 is/are rejected.

7) Claim(s) 5 and 11 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 07 June 2000 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.

4) Interview Summary (PTO-413) Paper No(s). _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because handwriting is difficult to read. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 5 and 11 are objected to because of the following informalities: Claim 5 and 11 recite the limitation "data content" in lines 1-2 of each of claims 5 and 11. The Examiner would like to point out that since "data content" is written in indefinite form in claims 5 and 11 that the claim language dictates that the "data content" in claims 5 and 11 is referring to an arbitrary data content used to identify "the data content of the identified data unit" already indicated in claim 1 and that "data content" in claims 5 and 11 is not "the data content of the identified data unit" as already indicated in claim 1. Because of the similarity in wording, the Examiner suggests using clarifying language or another term in claims 5 and 11 to avoid confusion.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Applicant teaches that the erroneous data verification parameter is used to verify the operation of the data verification circuitry and hence the data verification circuitry must carry out the operation of using the erroneous data verification parameter to verify data content of said identified data unit. Claim 1 cites, "data verification parameter does not verify data content of said identified data unit" which implies that the erroneous data verification is not carried out which contradicts the Applicant's disclosure, hence renders claim 1 non-enabling. [Emphasis Added, see below for additional remarks]

Claim 7 cites similar language as in claim 1.

Claims 2-6 and 8-12 depend from claim 1, hence inherit the deficiencies of claim 1.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-6 and 8-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 cites, "a data verification parameter

generator for generating an erroneous data verification parameter". The Examiner would like to point out that the name "data verification parameter generator" implies that a data verification parameter generator is a unit for producing a data verification parameter and not an erroneous data verification parameter. For example, on page 2 of the Applicant's specification, the Applicant teaches that a data verification parameter can be parity bits and hence one of ordinary skill in the art at the time the invention was made would interpret a "data verification parameter generator" to be a parity generator or encoder and not a circuit for producing erroneous data verification parameters. Hence, use of "data verification parameter generator" to indicate a circuit for producing erroneous data verification parameters renders claim 1 indefinite.

Claims 2-6 and 8-12 depend from claim 1, hence inherit the deficiencies of claim 1.

5. While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "data verification parameter generator" in claim 1 is used by the claim to mean "a circuit for producing erroneous data verification parameters," while the accepted meaning is "a circuit for producing data verification parameters." [Emphasis Added]

Claims 2-6 and 8-12 depend from claim 1, hence inherit the deficiencies of claim 1.

6. Claims 2-6 and 8-12 recites the limitation "said corresponding data verification parameter" in lines 6-7. There is insufficient antecedent basis for this limitation in the

claim. The Examiner is assuming that the Applicant intends, said corresponding erroneous data verification parameter. [Emphasis Added]

7. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "data verification parameter does not verify data content of said identified data unit" in claim 1 is used by the claim to mean "data verification parameter cannot be used to verify data content of said identified data unit," while the accepted meaning is the data verification parameter does not carry out the step of verifying.

Claim 7 cites similar language as in claim 1.

Claims 2-6 and 8-12 depend from claim 1, hence inherit the deficiencies of claim 1.

8. Claims 8-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8-12 recites the limitation "The method" in line 1 of each of the claims 8-12.

There is insufficient antecedent basis for this limitation in the claim.

9. The Examiner would like to point out that the current Application is replete with 35 U.S.C. 112 problems and that the Applicant should carefully review all claims for 35 U.S.C. 112 problems and make appropriate corrections.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Khan, Aurangzeb K. (US 4561095 A).

11. 35 U.S.C. 102(b) rejection of claim 1.

Khan teaches a test circuit for inclusion on an integrated circuit comprising (col. 3, lines 34-43, Khan): a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence (see X-Y ADDRESS DECODE circuit 18 in Figure 1 of Khan); and a circuit for generating an erroneous data verification parameter (ERROR INSERT DECODE circuit 32 in Figure 1 of Khan) corresponding to said data unit identified by said data unit identifier (the address of a data unit is clearly a data unit identifier for the data unit) so that said corresponding data verification parameter cannot be used to verify data content of said identified data unit (clearly, if an error is inserted into the parity coded word, the parity will not be able to establish the accuracy of the

word).

12. 35 U.S.C. 102(b) rejection of claims 2 and 3.

See col. 7, lines 3-15 in Khan.

13. 35 U.S.C. 102(b) rejection of claim 4.

See rejection to claim 1, above.

14. 35 U.S.C. 102(b) rejection of claim 5.

The Examiner would like to point out that since "data content" is written in indefinite form in claims 5 and 11 that the claim language dictates that the "data content" in claims 5 and 11 is referring to an arbitrary data content used to identify "the data content of the identified data unit" as already indicated in claim 1 and that "data content" in claims 5 and 11 is not "the data content of the identified data unit" as already indicated in claim 1.

An address is an arbitrary data content (see rejection to claim 1, above).

15. 35 U.S.C. 102(b) rejection of claim 6.

See X-Y ADDRESS DECODE circuit 18 in Figure 1 of Khan. Note; an address is a clear indication of position within a data stream and also position within a memory unit.

16. 35 U.S.C. 102(b) rejection of claim 7.

The limitations in claim 7 are substantially the same as in claim 1 except for the real time testing of a data receiver. The Apparatus of Figure 1 in Khan receives data bits Do-D4, hence is a data receiver. In lines 58-60 of column 15, Khan teaches that the deliberate insertion of an erroneous data bit is carried out in real-time.

17. 35 U.S.C. 102(b) rejection of claims 8 and 9.

See col. 7, lines 3-15 in Khan.

18. 35 U.S.C. 102(b) rejection of claim 10.

See rejection to claim 1, above.

19. 35 U.S.C. 102(b) rejection of claim 11.

The Examiner would like to point out that since "data content" is written in indefinite form in claims 5 and 11 that the claim language dictates that the "data content" in claims 5 and 11 is referring to an arbitrary data content used to identify "the data content of the identified data unit" as already indicated in claim 1 and that "data content" in claims 5 and 11 is not "the data content of the identified data unit" as already indicated in claim 1. An address is an arbitrary data content (see rejection to claim 1, above).

20. 35 U.S.C. 102(b) rejection of claim 12.

See X-Y ADDRESS DECODE circuit 18 in Figure 1 of Khan. Note; an address is a clear indication of position within a data stream and also position within a memory unit.

Conclusion

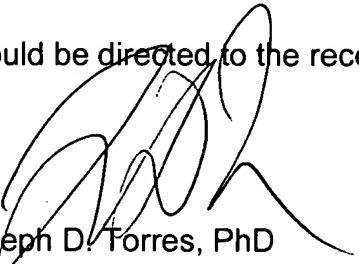
21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. P. N. CROCKETT ET AL (US 3465132 A) teaches circuits for handling intentionally mutated information. Dixon, Robert Christopher (US 5872790 A) teaches a method of simulating errors in the retrieval of information from a computer memory for testing an error detection or correction device. Kirk, David L. (US 4670876 A) teaches verification of error detection logic; namely, verification of parity generation and check logic. E. M. PRELL ET AL (US 3401379 A) teaches equipment for testing error detector circuits.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decay can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding
should be directed to the receptionist whose telephone number is (703)-746-7240.


Joseph D. Torres, PhD
Art Unit 2133
December 18, 2002


PHUNG M. CHUNG
PRIMARY EXAMINER